Rijksdienst voor Ondernemend Nederland

The Chips for Europe Initiative

BUILD INNOVATIVE ECO-SYSTEMS

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Noviotec Campus Nijmegen

ir. Jacob Jan de Boer
Advisor European Innovation Programmes

jacobjan.deboer@rvo.nl
+31 6 23 31 12 52

The innovation landscape

NATIONAL

CROSS BORDER COLLABORATION

NATIONAL

EUREKA

KDT-JU (CHIPS-JU)

HORIZON EUROPE

industry-led international communities focused on strategic technology areas that aim to meet market needs and solve economic, technological and societal challenges

Key Digital Technology Partnership 3A (AENEAS, EPoSS and Inside) represents industry in KDT

NATIONAL FUNDING

EUROPEAN FUNDING

# Fostering International Cooperation in R&D and Innovation Collaboration

EUREKA

› Eureka is the world's biggest public network for international cooperation in R&D and innovation present in over **45 countries**

› Trans-national programmes following **national priorities**

Annual budget
€ 20 mio (for the clusters)

EUROPEAN (CHIPS JU)

› Horizon Europe is the most open and by far the **largest research and innovation programme** globally. Association of non-EU countries to the programme is one of the key vehicles to ensure this openness.

› Innovation programmes following **European Strategy**

Annual budget
€ 35 mio (for the Chips JU)
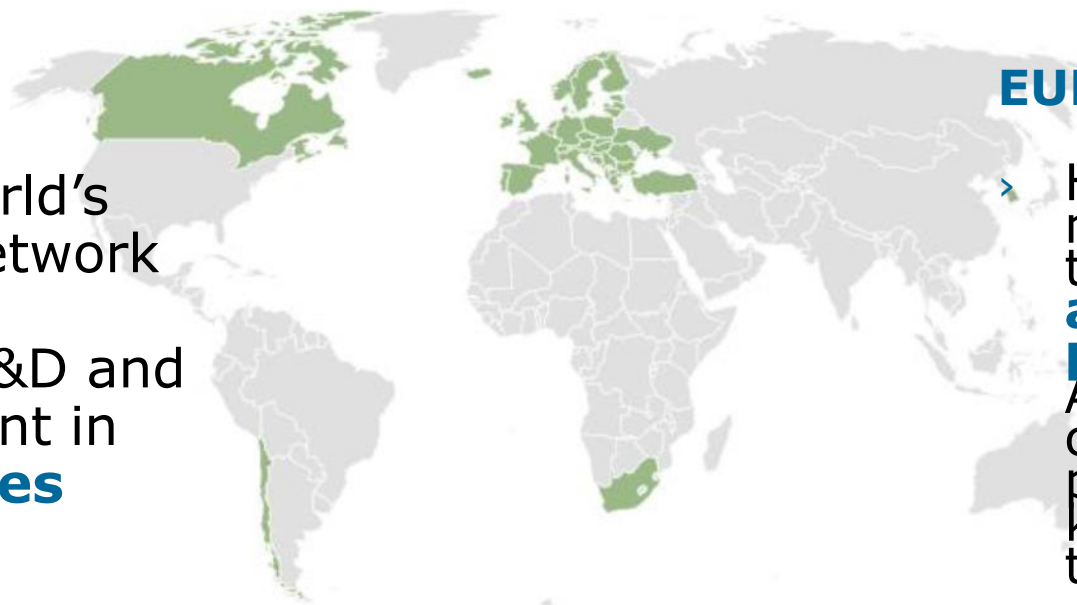
Differences between Eureka and Chips JU

EUREKA

› At least **two** participating countries

› Open to **47 Eureka countries** (and beyond)

› Mid-sized projects, agile (even SME can lead the project)

› Scope of the project defined by consortium - focus on national topics – **roadmaps HightechNL**

› **Only national funding** according to national rules

CHIPS JU

› At least **three** participating countries

› **Horizon Europe** associated countries

› Slightly larger projects (4 out of 5 projects have LE in the lead)

› Top-down approach - focus topics - **pan-European dimension**

› Follow **EU funding rules**

› Two-stage calls

› Industry in the lead ⇔ close-to-market RD&I

› ECS-SRIA facilitates the preparation of the future KDT and Xecs calls

› Dutch perspective: project needs to have a link to hightechNL roadmaps

Join us at one of the following events

INFORMATION SESSION EU CHIPS ACT NETHERLANDS SEMICON COMPETENCE CENTER

› 5 July

› Registration

› location: RVO Den Haag

XECS MATCHMAKING EVENT OF THE XECS CALL 3

› 25 September

› Registration

› location: France, Paris

ITEA PO PREPARATION DAYS

› 12 – 13 September

› registration

› location: Germany, Berlin

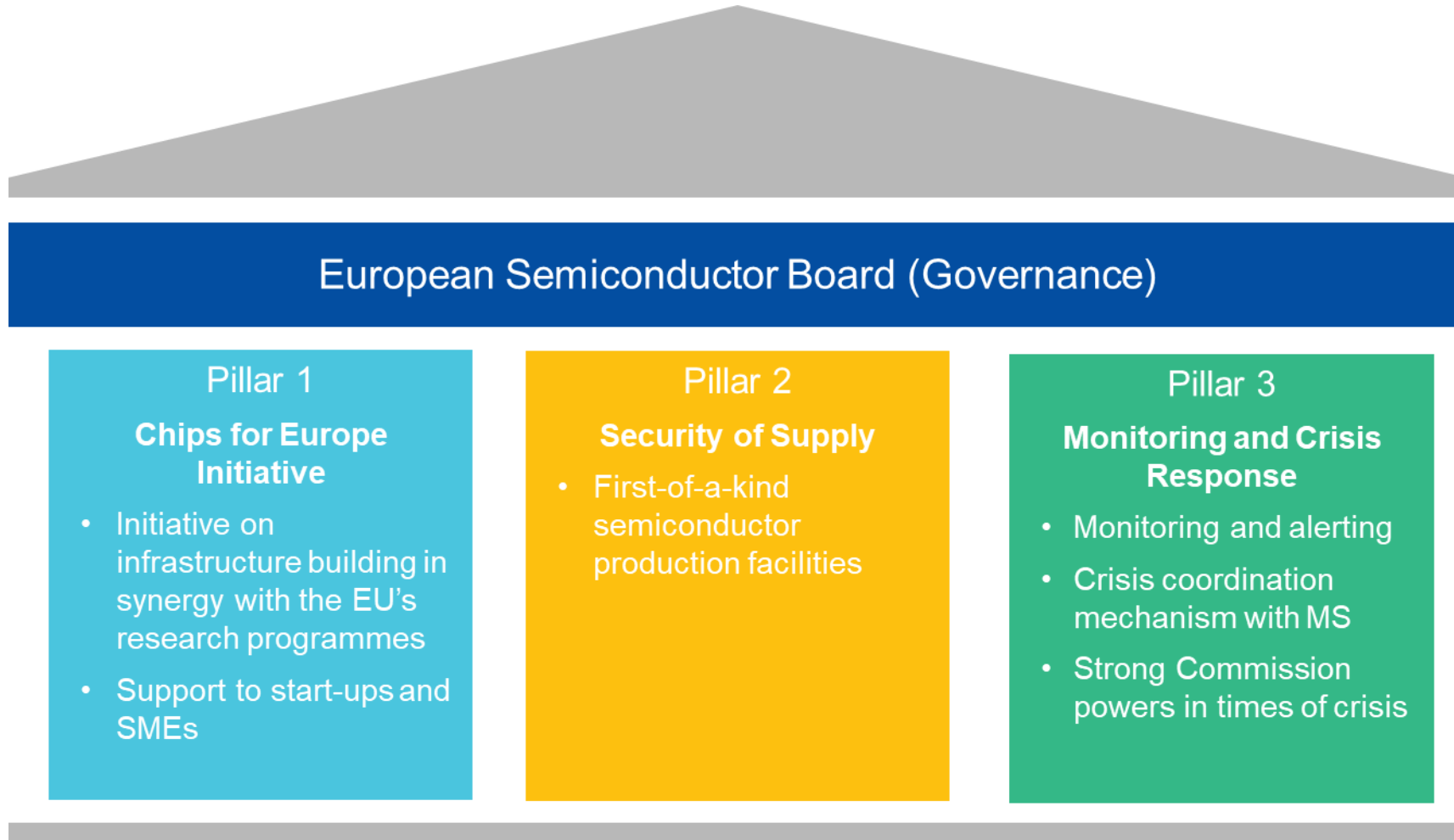**CHIPS JU LAUNCH EVENT**

› 22 – 23 November

› registration will open soon

› location: Belgium, tbc

Three pillars of the Chips Act

European Semiconductor Board (Governance)

Pillar 1

Chips for Europe Initiative

- Initiative on infrastructure building in synergy with the EU's research programmes
- Support to start-ups and SMEs

Pillar 2

Security of Supply

- First-of-a-kind semiconductor production facilities

Pillar 3

Monitoring and Crisis Response

- Monitoring and alerting
- Crisis coordination mechanism with MS
- Strong Commission powers in times of crisis

The Chips for Europe Initiative

1 Developing innovative eco-systems

2 Semiconductor competence centers

3 How to join?

Rijksdienst voor Ondernemend Nederland

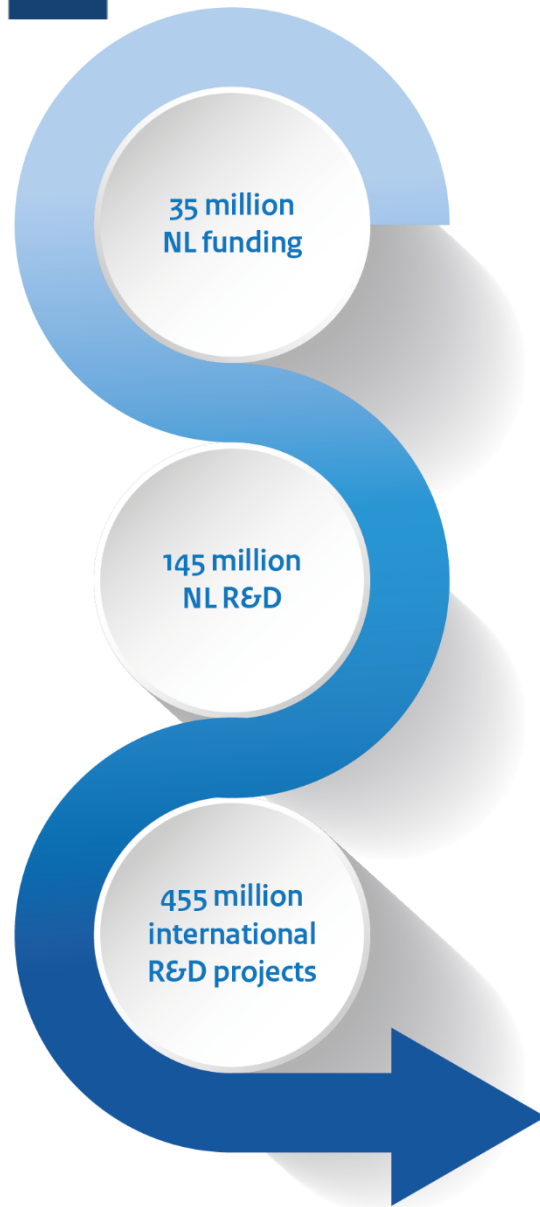# Developing innovative eco-systems

KDT JU is an EU-driven, public-private partnership, funding innovation in electronic components and systems

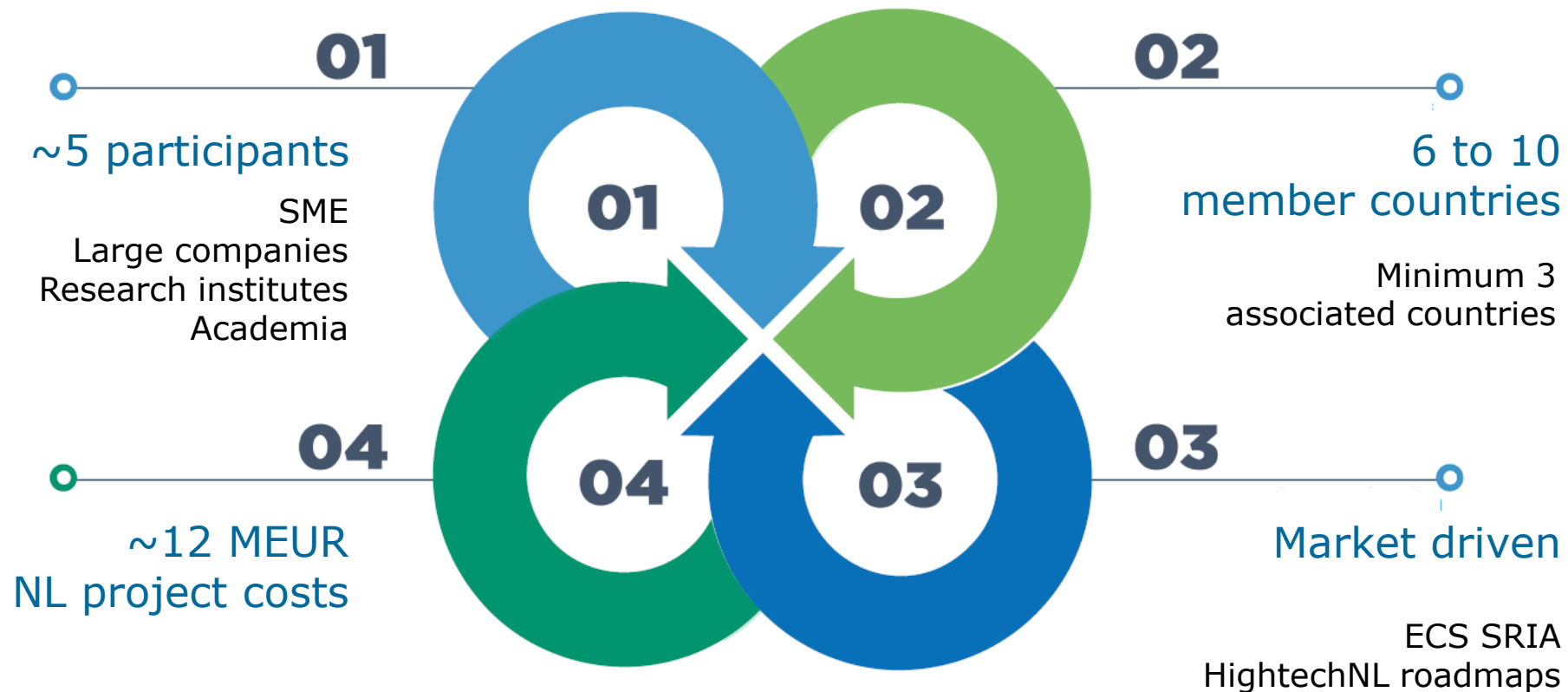# Collaborative innovation is a great multiplier

35 million
NL funding

145 million
NL R&D

455 million
international
R&D projects

National collaboration

62 participants

12 projects

42 companies (22 *SME and high-tech scale ups*)

International collaboration

390 participants

23 countries

A typical Dutch KDT consortium

01

~5 participants

SME
Large companies
Research institutes
Academia

02

**6 to 10
member countries**

Minimum 3
associated countries

04

**~12 MEUR
NL project costs**

03

Market driven

ECS SRIA
HightechNL roadmaps

Fostering ECS innovation in the Netherlands

FUNDING OUTLOOK

› SMEs, large companies and RTOs/academia are eligible for funding

› Budget limit per call: € 30 mio

› Maximum national funding for Dutch consortium

  – IA projects: € 10 mio

  – RIA project: € 5 mio

› Funding criteria: innovation, collaboration & impact

FUNDING RATES

activities	NL	EU
SME	30%	35%
Industry	20%	20%
Academia/RTO	25%	35%

› More information: Key Digital Technologies Joint Undertaking (KDT JU) (rvo.nl)

Competence Centers
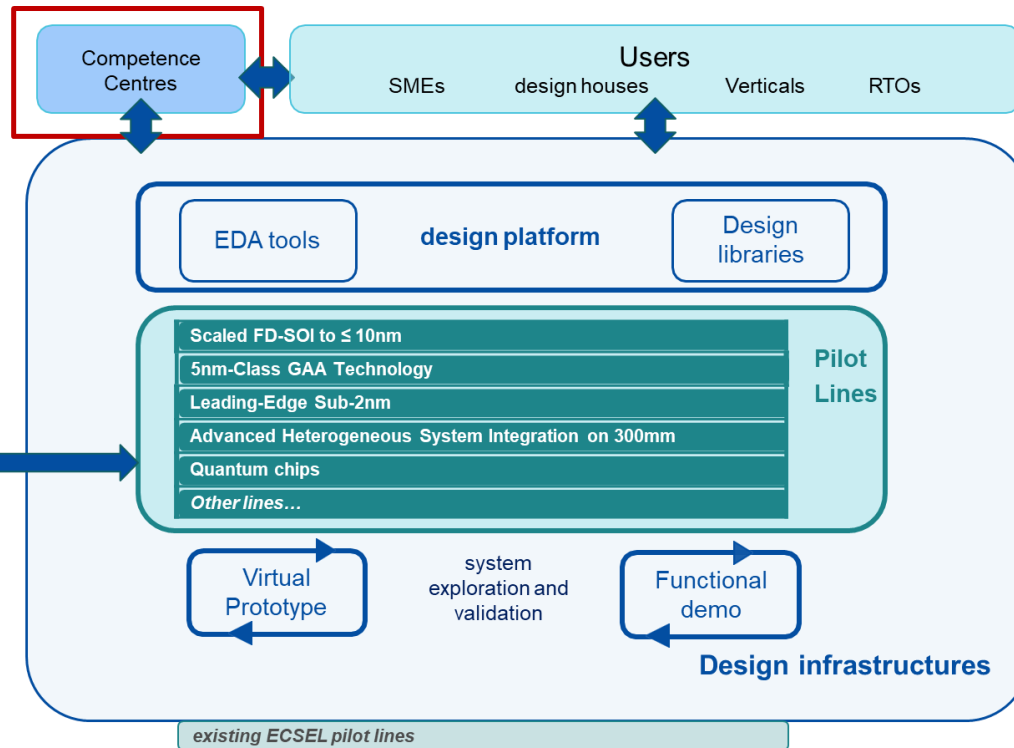
> › Competence centers will facilitate open, transparent, and non-discriminatory access to and effective use of the **design infrastructure** and the **pilot lines** They will become poles of attraction for **innovation and for new, highly skilled talent**

Objectives of the European Network of Competence Centers

FACILITATE ACCESS

1. strengthen capacities and offer a wide range of expertise to the stakeholders, including **end user SMEs and start ups**, facilitating access to and effective use of the capacities and facilities;

MOBILISING TALENT

› address the **skills shortage**, attracting and mobilising new talent and supporting the emergence of a suitably skilled workforce for strengthening the semiconductor sector, including via reskilling and upskilling of workers.

Competence Centers' Services & Activities

› Facilitating access to the design platform and to pilot lines

› Supporting interested stakeholders in developing semiconductor solutions (technology transfer)

› Providing (access to) training on skills

› Facilitating access to the European Network of Competence Centers

› Promoting the Chips Fund and facilitating access to venture capital

› Awareness raising, promoting services, promoting success stories

EU support for at least one centre per Member State	Co-investment with Member States and Regions	Supporting industry and public services
Access to design platform and pilot lines	Focus on Semiconductors Skills	A strong European network of Competence Centres

National specialization, e.g. photonics, quantum, materials & deposition, medical devices, automotive electronics, 6G

Network of Competence Centers

COMPETENCE CENTER CONSORTIUM

› Single organisation or coordinated group of organisations with complementary expertise

› Established with non-profit objective

› Aiming to promote the use of semiconductor technologies

› Can be built on established entities in the field or can be set up from scratch

› Independent

USERS

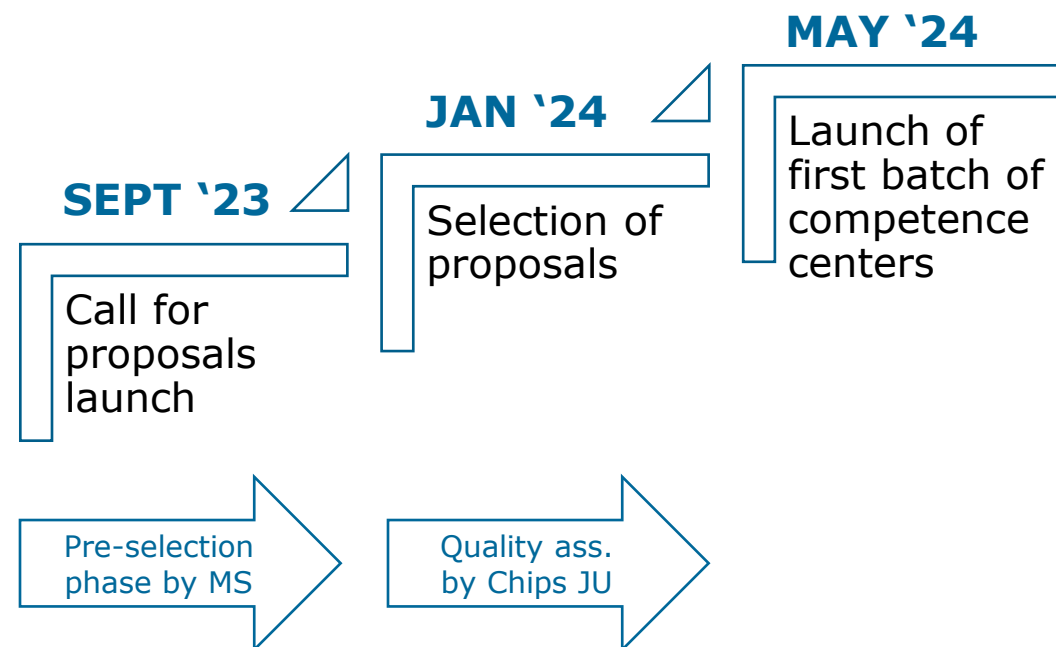› Companies, in particular local/national SMEs and startups, RTOs, academic institutions, public authorities
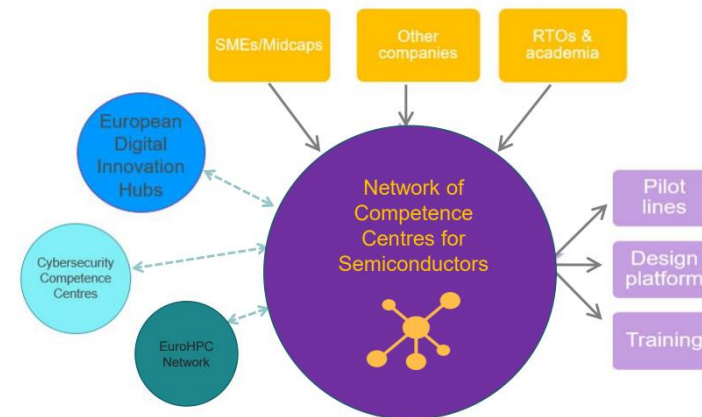
Selection process

FUNDING MODEL

› Member States are expected to co-finance their national competence centers on a 50-50 basis

› EU funding: max EUR 1 million per year, per country, for a 5-year period, provided that same or higher national co-financing is available

One competence center in the Netherlands

EXPECTED TIMELINE

SEPT '23
Call for proposals launch

JAN '24
Selection of proposals

MAY '24
Launch of first batch of competence centers

Pre-selection phase by MS →

Quality ass. by Chips JU →

Netherlands Semicon Competence Centers Information Session 5 July (3.00 – 5.30 pm)

› Current status of the EU Chips Act

› Activities and financing opportunities

› Selection procedure and planning

› More information and registration ([link](#))

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CONTACT

Rijksdienst voor Ondernemend
Nederland

rvo.nl/onderwerpen/internationaal-innoveren

robert-jaap.vanderbijl@rvo.nl

jacobjan.deboer@rvo.nl
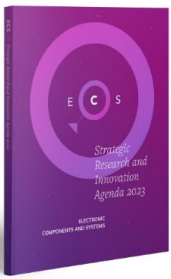
+31 6 21 83 94 77 (Bob)

+31 6 23 31 12 52 (Jacob Jan)

Linkedin.com/RVO

ECS-SRIA

ECS-SRIA is the basis for KDT JU and Xecs calls. It supports the ECS community to align innovation needs to support all major challenges within various application domains

› It's a living, open document that describes the top challenges and priorities in the field of electronic components and systems

› It's the go-to reference document for the KDT Work Programme

› It's updated annually to reflect market trends, industry dynamics, technology advancements, and long-term visions

› Updates are coordinated by AENEAS, EPoSS, and Inside
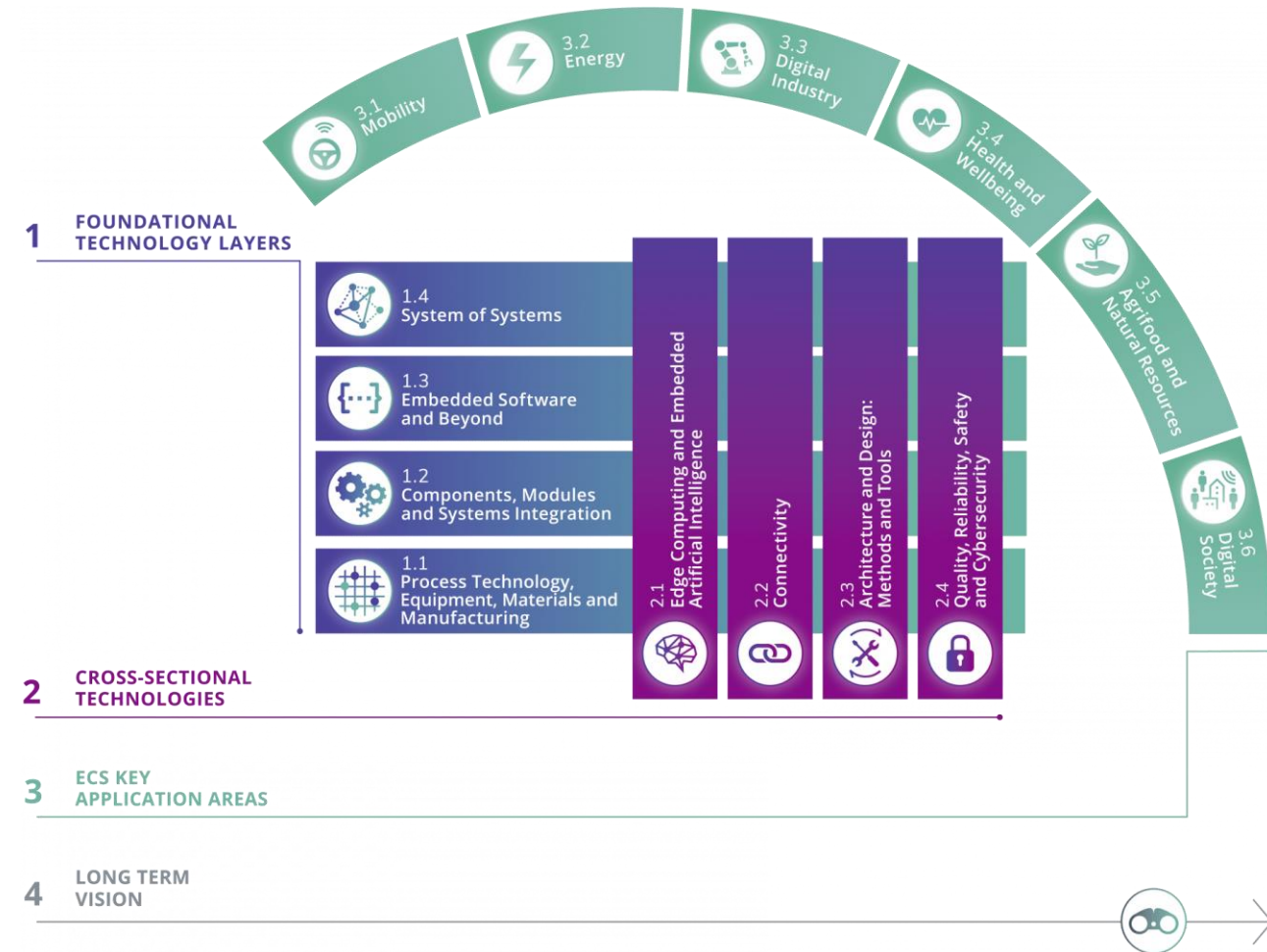
The draft version of the 2023 edition is available for download here.

The 6th edition can be downloaded from the ECS Collaboration Tool